

HCMOS/TTL COMPATIBLE VCXO IN HALF SIZE DIP PACKAGE- VC08 Series

FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Pulling Range
- Very Low Phase Jitter with Fundamental Crystal Design
- Commercial or Industrial Temperature Range, 5.0 V or 3.3 V Option
- Hermetically Sealed Half Size DIP Package with Industry Standard Lead Spacing

SPECIFICATIONS

Frequency Range 1 MHz to 39 MHz

Input Voltage (Vcc) $A = +5 \text{ VDC} \pm 5\%$; $B = +3.3 \text{ VDC} \pm 5\%$

Input Current 40 mA Maximum, depending on frequency and output load Control Voltage (Vc) $+2.5V \pm 2.0V$ for 5.0V part; $+1.65V \pm 1.5V$ for 3.3V part

Storage Temperature -55°C to 125°C

Frequency Stability / APR (Min) $A = \pm 50 / \pm 50$ ppm; $B = \pm 25 / \pm 50$ ppm; $C = \pm 50 / \pm 100$ ppm

Temperature Range

 $A = 0^{\circ}C$ to $70^{\circ}C$; $B = -40^{\circ}C$ to $85^{\circ}C$; $C = -10^{\circ}C$ to $60^{\circ}C$

Standard Stability / Pullability $AA = \pm 50 \text{ ppm} / 0^{\circ}\text{C}$ to 70°C , Absolute pull range (APR): $\pm 50 \text{ ppm}$ Minimum

0 = No Tristate 60/40% symmetry; 2 = No Tristate 55/45% symmetry **Duty Cycle**

4 = No Tristate 52.5/47.5% symmetry

Output Load HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates

Logic "1" / Logic "0" Level 0.9Vcc Minimum / 0.1Vcc Maximum Rise/Fall Time (Tr/Tf) 10 ns Maximum at 20% to 80% Vp-p

Start-up time 10 ms Maximum

Phase Jitter (RMS, 1 Sigma) 1 ps Maximum for fj > 1kHz; 0.3 ps Typical for fj = 12KHz to 20MHz

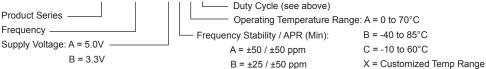
Modulation Bandwidth 10 kHz Minimum at -3 dB

Linearity / Slope ±10% Maximum of best straight line fit / Positive

Input Impedance 10 kOhms Minimum

Setability at Fnom, 25°C +2.5V ±0.5V for 5.0V part; +1.65V ±0.4V for 3.3V part





 $C = \pm 50 / \pm 100 \text{ ppm}$ $D = \pm 25 / \pm 75 \text{ ppm}$

OUTLINE DRAWING

