

HCMOS/TTL COMPATIBLE TRI-STATE VCXO IN CERAMIC LCC PACKAGE - VC53 Series

FEATURES

- RoHS Compliant (Pb-Free), Wide Frequency Pulling Range
- Very Low Phase Jitter with Fundamental Crystal Design
- Leadless Chip Carrier (LCC) Ultra Small Package with Industry de facto Standard Footprint
- Optional Enable/Disable Control at Either Pin #2 (VC53A) or Pin #5 (VC53B)

SPECIFICATIONS

Frequency Range 1 MHz to 108 MHz

Input Voltage (Vcc) $A = +5 \text{ VDC} \pm 5\%$; $B = +3.3 \text{ VDC} \pm 5\%$ **Input Current** 15 mA Max for 3.3V and 20 mA Max for 5V

Control Voltage (Vc) $+2.5V \pm 2.0V$ for 5.0V part; $+1.65V \pm 1.5V$ for 3.3V part

Storage Temperature -55°C to 125°C

Frequency Stability / APR (Min)

Temperature Range

 $A = \pm 50 / \pm 50 \text{ ppm}$; $B = \pm 25 / \pm 50 \text{ ppm}$; $C = \pm 50 / \pm 100 \text{ ppm}$; $D = \pm 25 / \pm 75 \text{ ppm}$

 $A = 0^{\circ}C$ to $70^{\circ}C$; $B = -40^{\circ}C$ to $85^{\circ}C$; $G = -10^{\circ}C$ to $70^{\circ}C$

Standard Stability / Pullability BA = ± 25 ppm / 0°C to 70°C, Absolute pull range (APR): ± 50 ppm Minimum

1 = Tristate 60/40% symmetry; 3 = Tristate 55/45% symmetry **Duty Cycle Output Load** HCMOS: drive up to 15 pF load; TTL: drive up to 10 TTL gates

Logic "1" / Logic "0" Level 0.9Vcc Minimum / 0.1Vcc Maximum 8 ns Maximum at 20% to 80% Vp-p Rise/Fall Time (Tr/Tf)

Start-up time 10 ms Maximum

Phase Jitter (RMS, 1 Sigma) 1 ps Maximum for fj > 1kHz; 0.4 ps Typical for fj = 12KHz to 20MHz

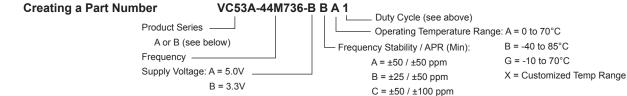
Modulation Bandwidth 12 kHz Minimum at -3 dB

Linearity / Slope ±10% Maximum of best straight line fit / Positive

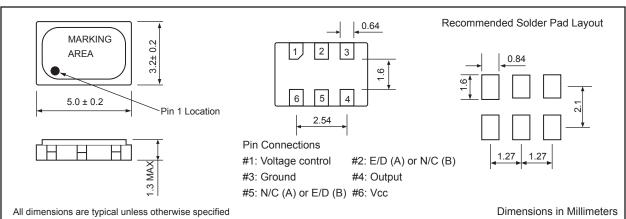
Input Impedance 10 kOhms Minimum

Setability at Fnom, 25°C +2.5V ±0.5V for 5.0V part; +1.65V ±0.4V for 3.3V part **Tristate Function** Input (Pin 2 or 5) High (> 2.2V) or open: Output (Pin 4) active Input (Pin 2 or 5) Low (< 0.5V): Output disabled in high impedance

Enable/Disable Time 100 ns Maximum



OUTLINE DRAWING



 $D = \pm 25 / \pm 75 ppm$